

# Chunghwa Picture Tubes, Ltd. Technical Specification

To : Date :

TFT LCD CLAA141WB02

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APPROVED BY	CHECKED BY	PREPARED BY									
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# **RECORD OF REVISIONS**

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# **1. OVERVIEW**

*CLAA141WB02*(with LVDS interface) is 14.1" color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, driver ICs, control circuit, and backlight.

By applying 6 bits digital data, 1280×800, 262K color images are displayed on the 14.1" diagonal screen. Input power voltage is single 3.3V for LCD driving.

Inverter for backlight is not included in this module. General specifications are summarized in the following table:

ITEM	SPECIFICATION						
Display Area(mm)	303.744(H) x 189.84.(V) (14.1-inch diagonal)						
Number of Pixels	1280 x 3(H) x 800(V)						
Pixel Pitch(mm)	0.2373(H) x 0.2373(V)						
Color Pixel Arrangement	RGB vertical stripe						
Display Mode	normally white TN						
Number of Colors	262144 colors						
Optimum Viewing Angle	6 o'clock						
Brightness(cd/m <sup>2</sup> )	200 (5 point average), lamp current 6mA(typ)						
Power consumption(W)	5.8W (typ)						
Module Size(mm)	319.5x205.5x5.5(max)						
Module Weight(g)	440(max)						
Backlight Unit	CCFL, 1 tube						
Surface Treatment Anti-Glare type ; Hardness: 3H							

[Note] : Sign "( )" means tentative value.

The LCD Products listed on this document are not suitable for use of aerospace equipment, submarine cables, nuclear reactor control system and life support systems. If customers intend to use these LCD products for above application or not listed in "Standard" as follows, please contact our sales people in advance.

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tool, Industrial robot, Audio and Visual equipment, Other consumer products.

\*1)

\*2)

#### ITEM SYMBOL MIN MAX. UNIT REMARK Power Supply Voltage for LCD -0.3 VCC 4.0 V VCC+0.3 LVDS input Voltage VIN -0.3 V VESDt -250 250 V Static Electricity \*1) VESDc -15 15 KV ICC Rush Current \*2) 2 А I<sub>RUSH</sub> --\*3)\*4) **Operation Temperature** \*3) 0 50 Top Storage Temperature \*3)\*4) \*3) -20 60 Tstg 1180 Starting Lamp Voltage V<u>sl</u> 0 V

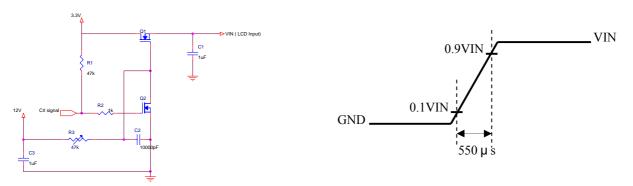
#### 2. ABSOLUTE MAXIMUM RATINGS

[Note] : \*1) Test Condition : IEC 1000-4-2,

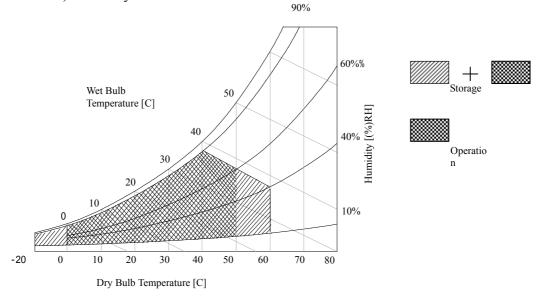
VESDt : Contact discharge to input connector

VESDc : Contact discharge to module

\*2) measure with below circuit, If Vcc rise time increase then  $I_{RUSH}$  decrease.







# **3. ELECTRICAL CHARACTERISTICS**

(A)TFT LCD

LCD						,	Ta = 25
ITEM		SYMBOL	MIN	ТҮР	MAX	UNIT	Remark
Power Supply Voltage for LCD		VCC	3.0	3.3	3.6	V	
Power Su	upply Current for LCD*1)	ICC	-	340	380	mA	
ICC Rush Current*2)		I <sub>RUSH</sub>			1.5	А	
T	Input Voltage	VIN	0	-	VCC	V	
Logic	Common Mode Voltage	VCM	1.125	1.25	1.375	V	
input Voltage	Differential Input Voltage	VID	250	350	450	mV	
voltage	Threshold Voltage(High)	VTH	-	-	100	mV	When
	Threshold Voltage(Low)	VTL	-100	-	-	mV	VCM = +1.2V
Toleran	ce of VID	ΔVID	-	-	35	mV	
Tolerance of VCM		ΔVCM	-	-	35	mV	

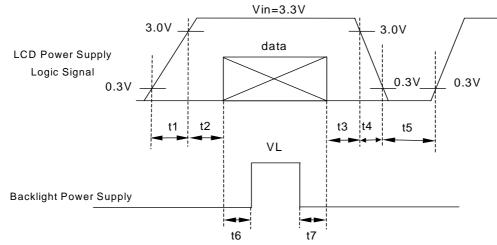
[Note] : \*1)Power Supply Current is in Gray0 63pattern and operation frequency is 71.1MHz(fV=60Hz).

\*2)Vin rise time is 550µsec

#### [Note 1]

- *VCC=3.3V*
- VCC turn on conditions :

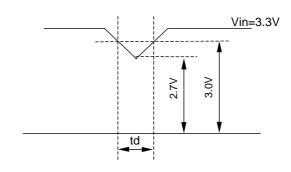
1 < t1	10ms	500 ms	t5
0 < t2	50 ms	300 ms	t6
0 < t3	50 ms	300 ms	t7
0 < t4	10 ms		



#### Data: RGB DATA, DCLK, HD, VD, DENA

- VCC dip conditions :
  - 1 ) When 2.7V VCC<3.0V, td 10 ms
  - 2) When VCC<2.7V

VCC dip conditions should follow VCC turn on conditions.

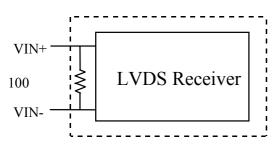


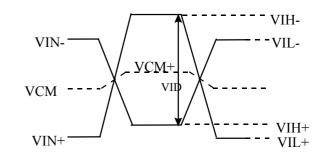
#### [Note 2]

- Typical value is measured when displaying horizontal gray scale line pattern 0~63 gray level 800 line mode
  - VCC = +3.3V
  - fCLKin=71.1MHz(fV=60Hz)

[Note 3]

• LVDS Signal definition :





 $VID = VIN_{+} - VIN_{-}$  $VCM = |VCM_{+} - VCM_{-}|$  $VID = |VID_{+} - VID_{-}|$  $VID_{+} = |VIH_{+} - VIH_{-}|$  $VID_{-} = |VIL_{+} - VIL_{-}|$  $VCM = (VIN_{+} - VIN_{-})/2$  $VCM_{+} = (VIH_{+} - VIH_{-})/2$  $VCM_{-} = (VIL_{+} - VIL_{-})/2$ 

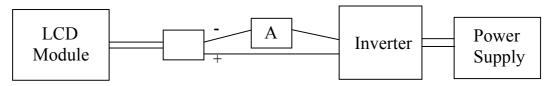
VIN<sub>+</sub> = Positive differential DATA & CLK Input VIN- = Negative differential DATA & CLK Input

#### (B) BACK LIGHT STSTEM

Ta=									
ITEM	SYMBOL	MIN	ТҮР	MAX	UNIT				
Lamp Voltage	VL	-	650	-	V				
Lamp Current *1)	IL	3.0	6.0	6.5	mA				
Inverter Frequency*3)	FI	50 -		60	KHz				
Lamp life time <b>*2</b> )	Life L	15,000	-	-	hr				
Starting $Ta = 0 *4$	Ma		-	1420	<b>X</b> 7				
$\begin{array}{c} \text{Lamp} \\ \text{Voltage} \end{array}  \text{Ta} = 25 \end{array}$	Vs		-	1180	V				

#### [Note 1]

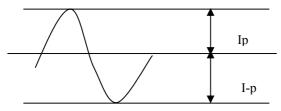
 \*1) Lamp Current measurement method ( The current meter is inserted in cold line) Standard inverter : SUMIDA IV11145T/AB2-LF, typical luminance = 200 cd/m<sup>2</sup> (5 point). The time that module luminance reduced to 50% of initial value. Base on Vs = (1180) V, Ta = 25°C, IL=6.0 mA continuous.



#### [Note 2]

Lamp frequency of inverter may produce interference with horizontal synchronous frequency, and this may cause horizontal beat on the display. Therefore, please adjust lamp frequency, and keep inverter as far from module as possible or use electronic shielding between inverter and module to avoid the interference.

The degrees of unbalance: less than 10% The ratio of wave height: less than  $\sqrt{2} \pm 10\%$ 



The degrees of umbalance = |Ip-I-p|/Irms\*100(%)The ratio of wave height = Ip(or I-p)/IrmsIp: lamp current high side peak, I-p: lamp current low side peak

# 4. INTERFACE CONNECTION

(a) CN1(Interface signal)

\* Connector type : FI - XB30SL - HF10 (JAE)

#### FI-X30HL (JAE,ROW Type)、FI-X30C2EL(JAE,COAXIAL Type)

<b></b>		
pin	Symbol	Function
1	VSS	Ground
2	VCC	+3.3V
3	VCC	+3.3V
4	V_EDID	DDC 3.3V Power
5	BIST	Panel BIST test
6	CLK_EDID	DDC Clock
7	DATA_EDID	DDC Data
8	R0M	LVDS Receiver Signal(-)—channel 0
9	ROP	LVDS Receiver Signal(+)—channel 0
10	Ground	Ground
11	R1M	LVDS Receiver Signal(-)-channel 1
12	R1P	LVDS Receiver Signal(+)—channel 1
13	Ground	Ground
14	R2M	LVDS Receiver Signal(-)—channel 2
15	R2P	LVDS Receiver Signal(+)—channel 2
16	Ground	Ground
17	RCLKM	LVDS Clock Signal(-)
18	RCLKP	LVDS Clock Signal(+)
19	Ground	Ground
20	NC	No Connect (Open)
21	NC	VCOM test provided, but customer-end unused; No Connect (open)
22	NC	No Connect (Open)
23	NC	No Connect (Open)
24	NC	No Connect (Open)
25	NC	No Connect (Open)
26	NC	No Connect (Open)
27	NC	No Connect (Open)
28	NC	No Connect (Open)
29	NC	No Connect (Open)
30	NC	No Connect (Open)
-		

Note: pin5 BIST Function: O(low) mean Normal Operation, 1(high) mean BIST Mode Enable

#### (b) CN2 (BACKLIGHT)

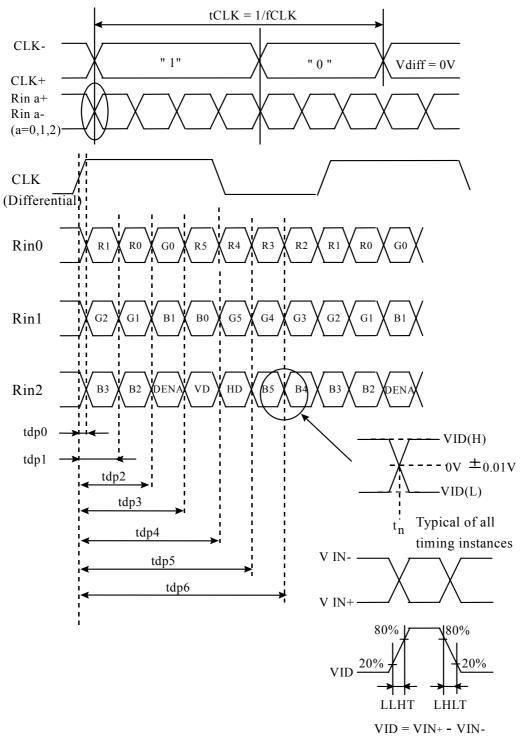
- Backlight-side connector: BHSR-02VS-1 (JST)
- Inverter-side connector: SM02B-BHSS-1(JST)

Pin No.	Symbol	Function						
1	СТН	VBLH (High voltage)						
2 CTL		VBLL (Low voltage)						
Netel VDI	$\mathbf{U} \mathbf{V} \mathbf{D} \mathbf{U} = \mathbf{V} \mathbf{I}$							

*[Note]* VBLH-VBLL = VL

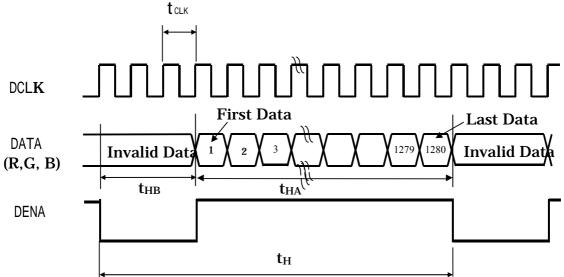
# **5. Input Signal Timing**

(a). LVDS (Rx) Input Signal Timing Chart

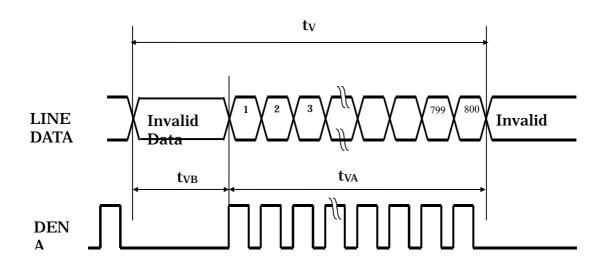


(b)LCD (Tx) Input Signal Timing Chart: (Rx output)

• Horizontal Timing:



• Vertical Timing



(c) Timing Specifications

							····	-
	Ι	TEM		SYMBOL	MIN	TYP	MAX	UNIT
	CLK frequ	iency		fCLKin	62.83	71.11	80.42	MHz
	CLK perio	od		tCLKin	12.43	14.06	15.92	ns
	LVDS Hig	h to Low trans	sition time	tLVT	—	0.75	1.5	ns
	LVDS Low	v to High trans	sition time	tLVT	—	0.75	1.5	ns
LVDS	Strobe pos	ition of Bit 0		tdp0	-0.4	0	0.4	ns
Input	Strobe pos	ition of Bit 1		tdp1	T/7-0.4	T/7	T/7+0.4	ns
Timing	Strobe pos	ition of Bit 2		tdp2	2T/7-0.4	2T/7	2T/7+0.4	ns
	Strobe pos		ition of Bit 3 f=71.1MHz		3T/7-0.4	3T/7	3T/7+0.4	ns
	Strobe pos	ition of Bit 4		tdp4	4T/7-0.4	4T/7	4T/7+0.4	ns
	Strobe pos	tion of Bit 5		tdp5	5T/7-0.4	5T/7	5T/7+0.4	ns
	Strobe pos	ition of Bit 6		tdp6	6T/7-0.4	6T/7	6T/7+0.4	ns
			Total	t <sub>H</sub>	1400	1440	1480	tCLK
LCD input		Horizonta	Active	t <sub>HA</sub>	1280	1280	1280	tCLK
signal			Blank	t <sub>HB</sub>	120	160	200	tCLK
	DENA		Frame Rate	fV	55	60	65	Hz
( LVDS Tx Input ,		Vertical	Tatol	t <sub>V</sub>	816	823	836	t <sub>H</sub>
Rx output )		vertical	Active	t <sub>VA</sub>	800	800	800	t <sub>H</sub>
<b>1</b> /			Blank	t <sub>VB</sub>	16	23	36	t <sub>H</sub>

 $VCC{=}3.3V$  , Ta=25

# [Note]

1 ) Data is latched at fall edge of DCLK in this specification.

2 ) DENA (Data Enable) should always be positive polarity as shown in the timing specification.

3) CLKIN should appear during all invalid period.

4) T(period) = 1/f

## (d) Color data definition

				RD	ATA					GΟ	ATA					ΒD	ATA		
Color	Input Data	R5	R4	R3	R2	R1	RO	G5	G4	G3	G2	G1	GO	B5	B4	B3	B2	B1	BO
		MSB					LSB	MSB					LSB	MSB					LSB
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
l Ē	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
l Ē	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Basic	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Color	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
i ľ	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
]	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	RED(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
[	RED(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
[	RED(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
RED													[]]]						
[	RED(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Green																			j
_	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	-	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Blue		ļ											; ;;					 	
		ļ		L				ļ					ļ			[]			
	Blue(62)		0	0	0		0	0		0	0		0	1	1	1	1	1	0
1	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

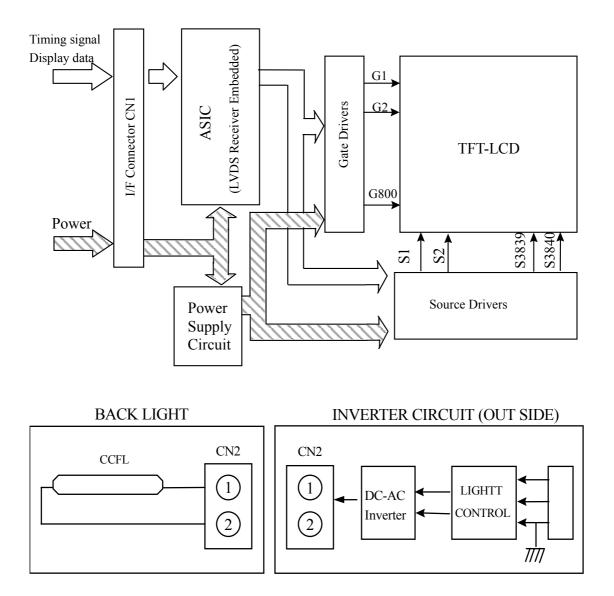
# [Note]

(1) Definition of gray scale: Color(n) : n means level of gray scale .

Bigger n means brighter level.

(2)Data : 1 = High, 0 = Low

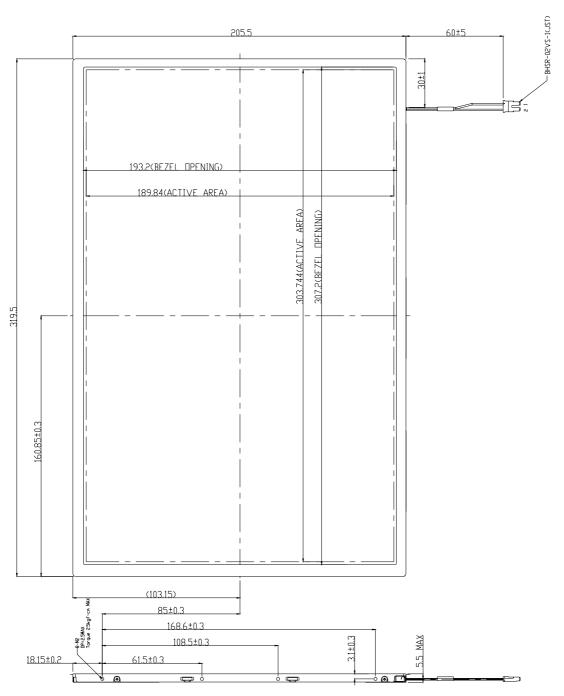
# 6. BLOCK DIAGRAM



# 7. MECHANICAL SPECIFICATION

(1) Front side

[Unit: mm]

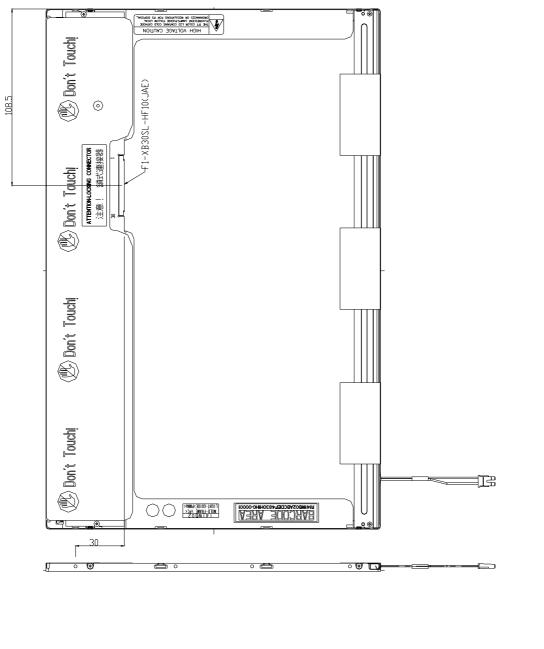


[Note] Undefined tolerances to be  $\pm 0.5$  mm

# CHUNGHWA PICTURES TUBES, LTD.,

#### (2) Rear side

[Unit: mm]



BHSR-02VS-1 (JST)

[Note] Undefined tolerances to be  $\pm 0.5$  mm

### 8. OPTICAL CHARACTERISTICS

Ta=25

item		symbol	condition	min	typ	max	un i t
contrast		CR	*1)	300	350		
5P Luminance		L	*3) I∟= 6 mA	160	200		cd/m <sup>2</sup>
5P Luminance Uniformity		ΔL	*4)			25	%
Response Time		Tr	*6)		5	20	ms
		Τf			11		ms
View angle	Horizontal	φ <sup>*2)</sup>	*2)CR 10	-35~35	-40 ~ 40		0
	Vertical	$\theta^{(2)}$		-35~15	-40 ~ 20		0
Crosstalk Ratio		CMR	*7)			1	%
Image sticking		tis	*8)			2	S
Color Temperature Coordinate	RED	х		0.559	0.589	0.619	
		у		0.296	0.326	0.356	
	GREEN	x		0.285	0.315	0.345	
		у	0 1 0	0.510	0.540	0.570	
	BLUE	х	$\Theta = \phi = 0^{\circ}$	0.123	0.153	0.183	
		У		0.095	0.125	0.155	
	WHITE	х		0.285	0.315	0.345	
		У		0.300	0.330	0.360	

#### [Note]

These items are measured using BM-5A(TOPCON)under the dark room condition( no ambient light) after more than 30 minutes from turning on the lamp unless noted.

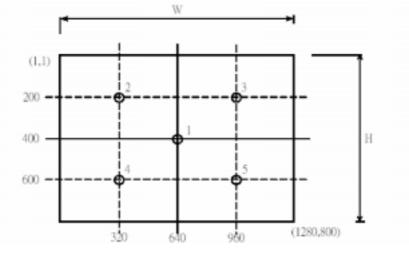
Condition: IL=6.0 mA, Inverter Frequency=50kHz. Inverter : SUMIDA IV11145T/AB2-LF Definition of these measurement items are as follows:

(1)Definition of Contrast Ratio : CR=ON(White)Luminance/OFF(Black)Luminance

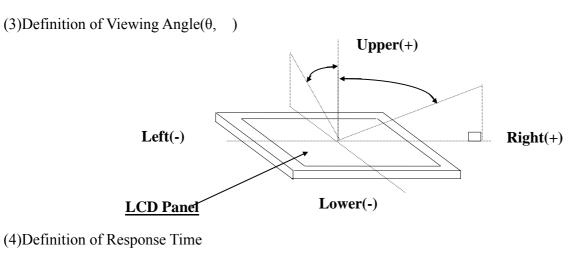
(2)Definition of Luminance and Luminance uniformity:

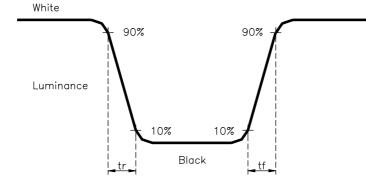
Measure White Luminance on the below center(1), 5 point(1,2,3,4.5)

5 and 13 point Uniformity :  $\Delta L = [(L_{MAX} - L_{MIN})/L_{MIN}] \times 100\%$ 



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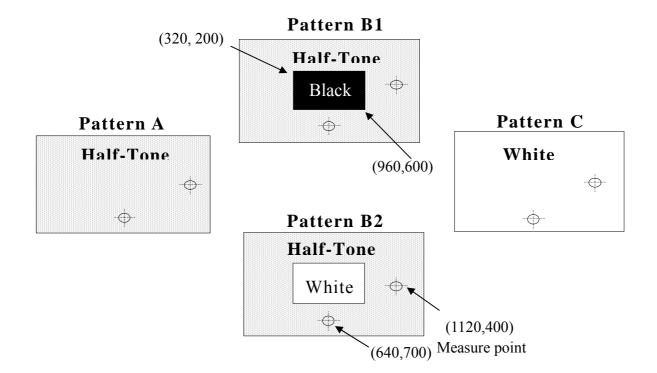
- (5)Definition of Contrast Ratio Uniformity  $CR = [CR(MAX) / CR(MIN) - 1] \times 100$
- (6)Definition of Luminance Uniformity  $L = [L(MAX) / L(MIN)-1] \times 100$

### (7) Definition of Cross talk Modulation Ratio

CTR= MAX((| (Lb1-La)/Lc | )×100, (| (Lb2-La)/Lc |)×100) La : Pattern A(Half-Tone pattern) Measure point Luminance

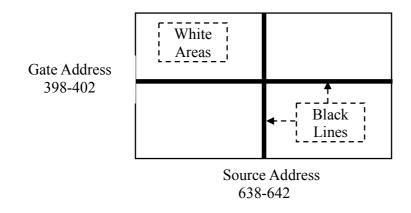
Lb1,Lb2 : Pattern B1, Pattern B2 Measure point Luminance

Lc: Pattern C(white pattern) Measure point Luminance



### (8)Definition of Image Sticking

Continuously display the test pattern shown in the figure below for two-hours. Then display a completely white screen. The previous image shall not persist more than two seconds at 25 .



# 9. RELIABILITY TEST CONDITIONS

#### (1)Temperature and Humidity

TEST ITEMS	CONDITIONS
HIGH TEMPERATURE OPERATION	50 ,250h
HIGH TEMPERATURE STORAGE	65 ,250h
LOW TEMPERATURE OPERATION	0 ,250h
LOW TEMPERATURE STORAGE	-25 ,250h
HIGH TEMPERATURE HIGH HUMIDITY OPERATION	40° C , 95% RH ,250h
HIGH TEMPERATURE HIGH HUMIDITY STORAGE	60 , 90%RH(Max), 48h
THERMAL SHOCK(No operation)	BETWEEN -25 (0.5h)AND 65 (0.5h),100 CYCLES

#### (2) Shock & Vibration

ITEMS	CONDITIONS		
SHOCK (NON-OPERATION)	<ul> <li>Shock level: 1980 m/s<sup>2</sup> (200G)</li> <li>Waveform: half sinusoidal wave, 2ms</li> <li>Number of shocks: one shock input in each direction of three mutually perpendicular axes for a total of six shock inputs.</li> </ul>		
VIBRATION (NON-OPERATION)	<ul> <li>Vibration level: 14.7 m/s<sup>2</sup> (1.5G), sinusoidal wave, perpendicular axis(each x,y,z axis: 0.5hr,</li> <li>Frequency range: 10 to 500 Hz</li> <li>Sweep speed : 0.5 octave / min</li> </ul>		

#### (3) ESD test

ITEMS	CONDITIONS		
	<ul> <li>Contact mode : 200pF, 0Ω, ±250V to I/F connector pins</li> <li>Air mode : 150pF, 330Ω, ±15KV to LCD glass and metal bezel</li> </ul>		

NOTE:test position(1)LCD glass and metal bezel (2)I/F connector pins

#### (4)Judgment standard

The judgment of the above test should be made as follow:

- Pass: Normal display image with no obvious non-uniformity and no line defect. Partial transformation of the module parts should be ignored.
- Fail: No display image, obvious non-uniformity, or line defects.

# **10. HANDLING PRECAUTIONS FOR TFT-LCD MODULE**

Please pay attention to the followings in handling- TFT-LCD products;

## **10.1 ASSEMBLY PRECAUTION**

- (1) Please use the mounting hole on the module side in installing and do not beading or wrenching LCD in assembling. And please do not drop, bend or twist LCD module in handling.
- (2) Please design display housing in accordance with the following guidelines.
- Housing case must be destined carefully so as not to put stresses on LCD all sides and not to wrench module. The stresses may cause non-uniformity even if there is no non-uniformity statically.
- Keep sufficient clearance between LCD module back surface and housing when the LCD module is mounted. Approximately 1.0 mm of the clearance in the design is recommended taking into account the tolerance of LCD module thickness and mounting structure height on the housing.
- When some parts, such as, FPC cable and ferrite plate, are installed underneath the LCD module, still sufficient clearance is required, such as 0.5mm. This clearance is, especially, to be reconsidered when the additional parts are implemented for EMI countermeasure.
- Design the inverter location and connector position carefully so as not to give stress to lamp cable, or not to interface the LCD module by the lamp cable.
- Keep sufficient clearance between LCD module and the others parts, such as inverter and speaker so as not to interface the LCD module. Approximately 1.0mm of the clearance in the design is recommended.
- (3) Please do not push or scratch LCD panel surface with any-thing hard. And do not soil LCD panel surface by touching with bare hands. (Polarizer film, surface of LCD panel is easy to be flawed.)
- (4) Please do not press any parts on the rear side such as source TCP, gate TCP, control circuit board and FPCs during handling LCD module. If pressing rear part is unavoidable, handle the LCD module with care not to damage them.
- (5) Please wipe out LCD panel surface with absorbent cotton or soft clothe in case of it being soiled.
- (6) Please wipe out drops of adhesives like saliva and water on LCD panel surface immediately. They might damage to cause panel surface variation and color change.
- (7) Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.
- (8) Please do not touch metal frames with bare hands and soiled gloves. A color change of the metal frames can happen during a long preservation of soiled LCD modules.
- (9) Please pay attention to handling lead wire of backlight so that it is not tugged in connecting with inverter.

# **10.2 OPERATING PRECAUTIONS**

- (1) Please be sure to turn off the power supply before connecting and disconnecting signal input cable.
- (2) Please do not change variable resistance settings in LCD module. They are adjusted to the most suitable value. If they are changed, it might happen LCD does not satisfy the characteristics specification.
- (3) Please consider that LCD backlight takes longer time to become stable of radiation characteristics in low temperature than in room temperature.
- (4) A condensation might happen on the surface and inside of LCD module in case of sudden change of ambient temperature.
- (5) Please pay attention to displaying the same pattern for very long time. Image might stick on LCD. If then, time going on can make LCD work well.
- (6) Please obey the same caution descriptions as ones that need to pay attention to ordinary electronic parts.

# **10.3 PRECAUTIONS WITH ELECTROSTATICS**

- (1) This LCD module use CMOS-IC on circuit board and TFT-LCD panel, and so it is easy to be affected by electrostatics. Please be careful with electrostatics by the way of your body connecting to the ground and so on.
- (2) Please remove protection film very slowly on the surface of LCD module to prevent from electrostatics occurrence.

## **10.4 STORAGE PRECAUTIONS**

- (1) When you store LCDs for a long time, it is recommended to keep the temperature between 0  $\sim$ 40 without the exposure of sunlight and to keep the humidity less than 90%RH.
- (2) Please do not leave the LCDs in the environment of high humidity and high temperature such as 60 90%RH.
- (3) Please do not leave the LCDs in the environment of low temperature; below -20 .

# **10.5 SAFETY PRECAUTIONS**

- (1) When you waste LCDs, it is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
- (2) If any liquid leaks out of a damaged-glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

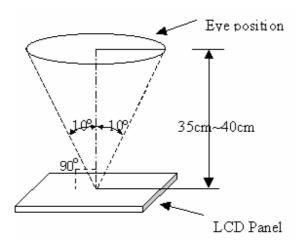
# 10.6 OTHERS

- (1) A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight Land strong UV rays.
- (2) Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.
- (3) For the packaging box, please pay attention to the followings:
- Packaging box and inner case for LCD are designed to protect the LCDs from the damage or scratching during transportation. Please do not open except picking LCDs up from the box.
- Please do not pile them up more than 3 boxes. (They are not designed so.) And please do not turn over.
- Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
- Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)

# **11. VISUAL INSPECTION SPECIFICATION**

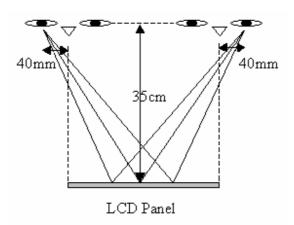
11.1 Inspection condition:

- (1) Viewing distance is approximately  $35 \sim 40$  cm.
- (2) Viewing angle is normal to the LCD panel as figure below( $10^{\circ}$ ).
- (3) Ambient temperature is approximately  $25 \pm 5$
- (4) Ambient humidity is  $60 \pm 5\%$  RH.
- (5) Ambient illumination is from  $300 \sim 500$  lux.
- (6) Input signal timing should be typical value.



11.2 Special condition

- (1) Viewing distance is close for inspection of adjacent dots and distance between defect dots.
- (2) Viewing condition of " Shot block non-uniformity from oblique angle" is as figure below.
- (3) Exceptional case: View angle  $\pm 40^{\circ}$  while inspected image-sticking.



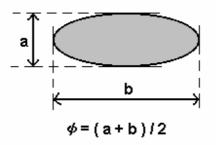
#### 11.3 Inspection Criteria

DEFECT TYPE			LIMIT	Note	
	SCRATCH		0.01mm W 0.05mm L 10mm	N 4	
VISUAL	INTERNAL	SPOT	0.15mm 0.5mm	N 4	*1)
DEFECT		FIBER	W 1.0mm, L 1.5mm	N 4	*1)
		POLARIZER BUBBLE	0.15mm 0.5mm	N 4	*1)
		TOTAL	N 8		
	BRIGHT DOT		N 4		*2)
	DARK DOT		N 5		
	TOTAL DOT		N 6		*2)
	TWO ADJACENT DOT		2 PAIR	*3)	
ELECTRICAL	THREE ADJACENT DOT		1 PAIRS		
DEFECT	FOUR OR MORE ADJACENT DOT		NOT ALLOWED		
	DISTANCE BETWEEN DEFECT DOT		Two bright dots	15mm	*4)
			Bright dot and dark dot	10mm	*4)
			Two dark dots	10mm	*4)
	LINE DEFECT		NOT ALLOV		
	MURA		5% ND FILTER		

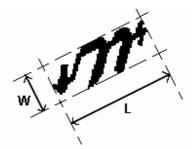
One pixel consists of 3 sub-pixels, including R,G, and B dot.(Sub-pixel = Dot) [Note]

\*1) W : Width[mm], L : Length[mm], N : Number,

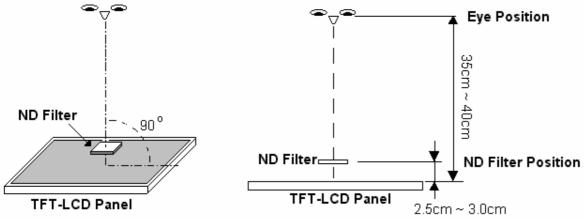
: Average Diameter



1. (White, black) Spot 2. Polarizer Bubble

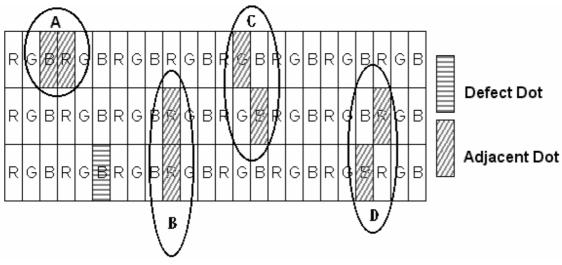


1. Fiber



\*2) Bright dot is defined through 5% transmission ND Filter as following.

\*3) Judge the defect dot and adjacent dot as following. Allow below (as A, B, C and D status) adjacent defect dots, including bright and dart adjacent dot. And they will be counted 2 defect dots in total quantity. The adjacent B status be not allow.



\*4) Definition of distance between defect dot as following.

